UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,401	04/15/2004	Du-Yeul Kim	SEC.1146	6396

20987 7590 04/09/2008

VOLENTINE & WHITT PLLC
ONE FREEDOM SQUARE
11951 FREEDOM DRIVE SUITE 1260
RESTON, VA 20190

EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
04/09/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,401	KIM, DU-YEUL	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 6-16* is/are rejected.

7)☒ Claim(s) *4 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Appeal Brief

In view of the Appeal Brief filed on December 19, 2007, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing at the end of this action.

OBJECTIONS

Claims

1. **Claims 1 and 6-8** are objected to because of the following informalities:

2. **As per claim 1**, on line 6, the **colon** should be replaced with a **semicolon** and the word “and” should be deleted.

3. **As per claim 6**, on line 5 the limitation "generating **a** first pipeline control signal" should instead read "generating **the** first pipeline control signal"

4. **Also per claim 6**, on line 7 the limitation "generating **a** second pipeline control signal" should instead read "generating **the** second pipeline control signal"

5. **As per claim 7**, the phrase "method of claim **5**" should instead read "method of claim **6**"

6. **As per claim 8**, the phrase "method of claim **5**" should instead read "method of claim **6**"

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. **Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.** The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 12 calls for the first delay (i.e. amount of time the first pipeline control signal is delayed from the clock signal) to be larger than the second delay (i.e. amount of the second pipeline control signal is delayed from the clock signal). However, having the first delay be larger than the

second delay is not disclosed anywhere in Applicant's specification or drawings. In fact, Applicant's drawings disclose the exact opposite situation (i.e. the second delay is larger than the first delay). Take for example Fig. 7 of Applicant's drawings. The amount of time the first pipeline control signal ("FRP") is delayed from the internal clock signal ("PCLK") (i.e. the first delay) is **less** than the amount of time the second pipeline control signal ("SRP") is delayed from PCLK (i.e. the second delay). In other words, the second delay is larger than the first delay. This makes perfect sense because the dependency relationship between signals PCLK, FRP, and SRP. FRP is directly dependent on PCLK (see Fig. 6). SRP is directly dependent on both PCLK and FRP (see Fig. 6). Therefore, because of the dependency SRP has on FRP, there is no way that SRP can be activated before FRP is activated. Accordingly, if the first delay is larger than the second delay that would mean that SRP is activated before FRP is activated, however, that situation is not possible as detailed above. For the purposes of applying art to the instant application, the Examiner will interpret the claim language of claim 12 to disclose the second delay is larger than the first delay.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. **Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.** As detailed in the 112, first paragraph rejection above, it is not possible for the first delay to be larger than the second delay. Therefore, the limitation "the first delay is larger than the second delay"

is vague and indefinite. For the purposes of applying art to the instant application, the Examiner will interpret the claim language of claim 12 to disclose the second delay is larger than the first delay.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-3, 6-10, and 12-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Toda (U.S. Patent 6,363,465) (hereinafter "Toda-465").

13. **As per claim 1**, Toda-465 discloses a pipeline memory device comprising:

a plurality of memory cells that store data (col. 10, lines 45-46; Fig. 2, element 12);

a data transfer path on which the data is transferred (col. 10, lines 38-41; Fig. 1);

a data fetching control circuit (col. 10, lines 50-54; Fig. 2, element 24) that is configured to generate:

a first pipeline control signal, in response to a first clock signal for generating the first pipeline control signal (col. 20, line 63 – col. 21, line 3; Figs. 18A and 18B; Figs. 19A and 19B, elements "CLK/CLK0" and "CK0"); *It should that the external clock signal "CLK/CLK0" is analogous to the "first clock signal" and "CK0" is analogous to the "first*

pipeline control signal." It should also be noted that when taking the circuits from Figs. 18A and 18B and using those circuits to generate "CK0" as illustrated in Figs. 19A and 19B, the signal "P1" is always high and the signal "CK0" is a don't care, as explained in col. 20, line 63 - col. 21, line 3.

a second pipeline control signal, in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal (col. 20, lines 41-48 and 54-63; Figs. 18A and 18B; Figs. 19A and 19B, elements "CL1", "CK0", and "CK1"); *It should be noted that "CL1" is analogous the "second clock signal" and "CK1" is analogous to the "second pipeline control signal." It should also be noted that when taking the circuits from Figs. 18A and 18B and using those circuits to generate "CK1" as illustrated in Figs. 19A and 19B, the signal "CLK" is replaced with the signal "CL1", as explained in col. 20, lines 61-63.*

a first pipeline stage which latches the data on the data transfer path in response to the first pipeline control signal (col. 15, lines 45-55; Fig. 8B, elements "S0" and "CK0"); *It should be noted that "S0" is analogous to the "first pipeline stage."*

a second pipeline stage which latches the data latched by the first pipeline stage in response to the second pipeline control signal (col. 15, lines 45-55; Fig. 8B, elements "S1" and "CK1"); *It should be noted that "S1" is analogous to the "second pipeline stage."*

and a third pipeline stage which outputs the data latched by the second pipeline stage to a data output pad in response to a data output clock signal (col. 15, lines 45-55; Fig. 8B, elements "S2" and "CK2"; Fig. 2, element 21; Figs. 19A and 19B). *It should*

be noted that when m=2, "S2" is analogous to the "third (and final) pipeline stage" where the data Dout is outputted. It should also be noted that "CK2" is analogous to the "data output clock signal."

14. **As per claim 2**, Toda-465 discloses the data fetching control circuit comprises:

a first edge trigger delay circuit which receives the first clock signal for generating the first pipeline control signal and generates the first pipeline control signal (col. 20, lines 50-53; col. 20, line 63 – col. 21, line 3; Figs. 18A and 18B, elements 29 and 32; Figs. 19A and 19B, elements "CLK/CLK0" and "CK0"); *As noted above, when taking the circuits from Figs. 18A and 18B and using those circuits to generate "CK0" as illustrated in Figs. 19A and 19B, the signal "P1" is always high and the signal "CK0" is a don't care, as explained in col. 20, line 63 - col. 21, line 3. Thus, "CK0" is obtained by buffering "CLK/CLK0" through NAND gates 29 and 32. Accordingly, NAND gates 29 and 32 are analogous to the "first edge trigger delay circuit."*

and a multiplexer which receives the second clock signal for generating the second pipeline control signal and the first pipeline control signal, and generates the second pipeline control signal (col. 20, lines 41-48 and 54-63; Figs. 18A and 18B, element 32; Figs. 19A and 19B, elements "CL1", "CK0", and "CK1"). *It should be noted that NAND gate 32 receives a buffered version of "CK0" and a buffered version of "CL1" and generates "CK1." Thus, NAND gate 32 is analogous to Applicant's "multiplexer."*

15. **As per claim 3**, Toda-465 discloses the first edge trigger delay circuit comprises an even number of inverters in a chain (col. 20, lines 50-53; col. 20, line 63 – col. 21, line 3; Fig. 18A, elements 29 and 32). *It should be noted that a NAND gate is logically*

equivalent to an inverter connected to the output of an AND gate. Thus, NAND gates 29 and 32 are logically equivalent to a first inverter connected to the output of a first AND gate and a second inverter connected to the output of a second AND gate. Accordingly, NAND gates 29 and 32 comprise an even number of inverters (2 inverters) in a chain.

16. **As per claim 6**, Toda-465 discloses a data fetching method for a pipeline memory device, comprising:

transferring data stored in memory cells along a transfer path (col. 10, lines 38-41 and 50-54; Fig. 1; Fig. 2, element 24);

generating a first pipeline control signal in response to a first clock signal for generating the first pipeline control signal (col. 20, line 63 – col. 21, line 3; Figs. 18A and 18B; Figs. 19A and 19B, elements “CLK/CLK0” and “CK0”); *See the citation note for the similar limitation in claim 1 above.*

generating a second pipeline control signal in response to a second clock signal for generating the second pipeline control signal and the first pipeline control signal (col. 20, lines 41-48 and 54-63; Figs. 18A and 18B; Figs. 19A and 19B, elements “CL1”, “CK0”, and “CK1”); *See the citation note for the similar limitation in claim 1 above.*

latching the data to a first pipeline stage on the transfer path in response to the first pipeline control signal (col. 15, lines 45-55; Fig. 8B, elements "S0" and “CK0”); *See the citation note for the similar limitation in claim 1 above.*

latching the data to a second pipeline stage on the transfer path in response to the second pipeline control signal (col. 15, lines 45-55; Fig. 8B, elements "S1" and "CK1"); *See the citation note for the similar limitation in claim 1 above.*

and outputting the data from the second pipeline stage to a data output pad in response to a data output clock signal (col. 15, lines 45-55; Fig. 8B, elements "S2" and "CK2"; Fig. 2, element 21; Figs. 19A and 19B). *See the citation note for the similar limitation in claim 1 above.*

17. **As per claim 7**, Toda-465 discloses a point of activation of the second pipeline control signal is determined depending on a point of activation of the first pipeline control signal (col. 20, lines 13-14; Fig. 17). *It should be noted that CK1's point of activation depends on CK0's point of activation because CK0 must be activated first in order for CK1 to be activated at some point in time later.*

18. **As per claim 8**, Toda-465 discloses the second pipeline control signal is activated when the first pipeline control signal is inactive (Fig. 17, elements "CK0" and "CK1").

19. **As per claim 9**, Toda-465 discloses an apparatus comprising:

at least one memory cell (col. 10, lines 45-46; Fig. 2, element 12);

a first pipeline stage coupled to the output of the at least one memory cell, wherein the first pipeline stage is driven by a first control signal (col. 15, lines 45-55; Fig. 8B, elements "S0" and "CK0"); *It should be noted that "S0" is analogous to the "first pipeline stage" and that "CK0" is analogous to the "first control signal."*

and a second pipeline stage coupled to the output of the first pipeline stage, wherein the second pipeline stage is driven by the first control signal and a second control signal (col. 15, lines 45-55; Fig. 8B, elements "S1" and "CK1"; col. 20, lines 41-48 and 54-63; Figs. 18A and 18B; Figs. 19A and 19B, elements "CK0" and "CK1"); *It should be noted that "S1" is analogous to the "second pipeline stage" and that "CK1" is analogous to the "second control signal." It should also be noted that signal CK0 drives signal CK1 and in turn signal CK1 drives S1. Therefore, it follows that signals CK0 and CK1 drive S1.*

20. **As per claim 10**, Toda-465 discloses the first control signal and the second control signal are driven by a clock signal (col. 20, line 41 – col. line 3; Figs. 18A and 18B; Figs. 19A and 19B, elements "CLK/CLK0", "CK0", and "CK1"). *It should be noted that external clock signal CLK0 drives CK0 and in turn CK0 drives CK1. Therefore, it follows that external clock signal CLK0 drives CK0 and CK1.*

21. **As per claim 12**, Toda-465 discloses the first control signal is delayed from the clock signal by a first delay (col. 16, lines 43-46; Fig. 17, elements "CLK" and "CK0"); *It should be noted that CK0 has **substantially** the same timing as the external clock signal CLK rather than the exact same timing as the external clock signal CLK. Therefore, it follows that CK0 is delayed from CLK by a finite amount of time (even if this amount of time is extremely small).*

and the second control signal is delayed from the clock signal by a second delay (Fig. 17, elements "CLK" and "CK1").

22. **As per claim 13**, Toda-465 discloses the second delay is larger than the first delay (Fig. 17, elements “CLK”, “CK0”, and “CK1”). *See the 112, first and second paragraph rejections of claim 13 above.*

23. **As per claim 14**, Toda-465 discloses the first control signal and the second control signal are never in an active state at the same time (Fig. 17, elements “CK0” and “CK1”).

24. **As per claim 15**, Toda-465 discloses the second pipeline stage is driven by the first control signal and the second control signal utilizes a multiplexer (col. 15, lines 45-55; Fig. 8B, elements "S1" and “CK1”; col. 20, lines 41-48 and 54-63; Figs. 18A and 18B; Figs. 19A and 19B, elements “CL1”, “CK0”, and “CK1”). *As noted above, signal CK0 drives signal CK1 and in turn signal CK1 drives S1. Therefore, it follows that signal CK0 drives S1 as well. Also as noted above, NAND gate 32 receives a buffered version of “CK0” and a buffered version of “CL1” and generates “CK1.” Thus, NAND gate 32 is analogous to Applicant's "multiplexer."*

25. **As per claim 16**, Toda-465 discloses the second pipeline stage is driven by the first control signal and the second control signal utilizes a NAND gate (col. 15, lines 45-55; Fig. 8B, elements "S1" and “CK1”; col. 20, lines 41-48 and 54-63; Figs. 18A and 18B; Figs. 19A and 19B, elements “CL1”, “CK0”, and “CK1”). *See the citation notes for claim 15 above.*

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toda-465 in view of Toda (U.S. Patent 6,449,727) (hereinafter "Toda-727").

28. **As per claim 11**, Toda-465 discloses all the limitations of claim 13 except the clock signal is an internal clock signal.

Toda-727 discloses generating an internal clock signal from an external clock signal (col. 16, lines 5-9).

Toda-465 and Toda-727 are analogous art because they are from the same field of endeavor, that being At the time of the invention it would have been obvious to a person of ordinary skill in the art to convert use Toda-727's internal clock signal generating circuits to convert Toda-465's external clock signal "CLK" into a master internal clock signal because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by know methods with no change in their respective functions, and the combination would have yielded the predictable results of allowing a memory controller to compensate for a difference between the timings of transfer data resulting from a difference between environments such as a difference between the numbers of memory modules. Consequently, high-speed synchronous data transfer is realized.

Therefore, it would have been obvious to combine Toda-465 and Toda-727 for the benefit of obtaining the invention as specified in claim 11.

Response to Arguments

29. Applicant's arguments with respect to **claims 1-3 and 6-16** in the Appeal Brief dated December 19, 2008 have been considered but are moot in view of the new grounds of rejection above.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

Allowable Subject Matter

30. **Claims 4 and 5** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims Rejected in the Application

31. Per the instant office action, **claims 1-3 and 6-16** have received a first action on the merits and are subject of a first action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 5,796,675 (Jang) discloses a synchronous memory device having dual input registers of pipeline structure capable of processing data at a high speed in a read path of the memory device.

2. U.S. Patent 5,802,596 (Shinozaki) discloses a high speed synchronous DRAM having a pipeline structure.

3. U.S. Patent 6,160,754 (Suh) discloses a synchronous memory device of a wave pipeline structure.

4. U.S. Patent 6,633,995 (Nam) discloses a system for generating N pipeline control signals by delaying at least one control signal corresponding to a subsequent data path circuit.

5. U.S. Patent 6,856,270 (Farmer et al.) discloses a pipeline array includes a register, a pipeline clock input, and Narrow Pulse Triggered Latches (NPTL) stages connected in series.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571)272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/
Examiner, Art Unit 2185
April 3, 2008

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185